Spartan-6 FPGA Speed File Changes

XCN11028 (v1.0) October 17, 2011

Customer Notification – For Your Information

Overview

Thank you for designing with the Xilinx Spartan®-6 FPGA family of devices. The purpose of this notification is to inform Xilinx customers of changes to the Spartan-6 FPGA speed files in the ISE® Design Suite v13.3 and later. The changes correct the speed files to match the values that have been shown in the data sheet.

Description

The DCM Phase Offset CLKIN_CLKFB_PHASE max value is being increased for all Spartan-6 FPGA speed grades. The block RAM maximum frequency F_{MAX} is being decreased for the lower power Spartan-6 -1L devices. The new speed files in the ISE v13.3 tools are v1.20 for the standard voltage devices and v1.08 for the lower power -1L devices. In addition, the block RAM F_{MAX} is being improved in the data sheet for the -2 speed grade. The following describes the details of these changes.

DCM Phase Offset CLKIN_CLKFB_PHASE

The DCM Phase Offset CLKIN_CLKFB_PHASE max value is being increased as shown in Table 1. When the DLL part of the DCM is used with clock feedback, CLKIN_CLKFB_PHASE describes the phase offset between the CLKIN and CLKFB inputs, and is reported as Phase Error in timing analysis. These new speed file values match the values that have been shown in the Spartan-6 FPGA Data Sheet, Table 54, Switching Characteristics for the Delay-Locked Loop (DLL).

Table 1: **DCM CLKIN_CLKFB_PHASE (CLK_FEEDBACK=1X) in Speed File**

ISE Design Suite Version	Speed File	-3 (-3Q)	-3N	-2 (-2Q)	Speed File	-1L
v13.2 and earlier	v1.19 and earlier	±50 ps	±60 ps	±60 ps	v1.07 and earlier	±150 ps
v13.3 and later	v1.20 and later	±150 ps	±150 ps	±150 ps	v1.08 and later	±250 ps

Designs that might be affected should be evaluated to confirm that they meet timing. Timing analysis can be run in ISE 13.3 software, or a speed file patch can be applied to run analysis on an earlier software version. To receive the patch, please reference Design Advisory Answer Record 44193.

Note that the data sheet specification for CLKIN_CLKFB_PHASE is 100 ps higher when CLK_FEEDBACK=2X. However, the speed file does not differentiate between 1X and 2X feedback, so the value for CLK_FEEDBACK=1X is used. Customers using 2X feedback should account for the extra 100 ps in their timing analysis. A footnote has been added to the Spartan-6 FPGA Data Sheet v3.0 to note that the 2X feedback value must be manually accounted for in timing analysis. See Table 2.

Table 2: **DCM CLKIN_CLKFB_PHASE in Data Sheet**

Condition	-3 (-3Q)	-3N	-2 (-2Q)	-1L
CLK_FEEDBACK=1X	±150 ps	±150 ps	±150 ps	±250 ps
CLK_FEEDBACK=2X(1)	±250 ps	±250 ps	±250 ps	±350 ps

Notes:
1. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Block RAM Maximum Frequency F_{MAX}

The block RAM maximum frequency F_{MAX} is being reduced for the lower power Spartan-6 -1L device speed grade from 250 MHz to 150 MHz. Customers using block RAM in the -1L devices should limit their clock frequencies to 150 MHz, re-run timing analysis using the ISE v13.3 tools, or re-run timing analysis using an earlier version of the ISE tools with the patch applied from Design Advisory Answer Record 44192.

The block RAM F_{MAX} is being improved for the -2 speed grade from 260 MHz to 280 MHz in the Spartan-6 FPGA Data Sheet v3.0. The speed file specification has been 280 MHz since the -2 speed grade was improved in the ISE v12.4.1 update. No customer action is required and no software updates are needed for this change.

Table 3 summarizes the block RAM F_{MAX} changes.

Table 3: **Block RAM F_{MAX}**

ISE Design Suite Version	Speed File	-3 (-3Q)	-3N	-2 (-2Q)	Speed File	-1L
v13.2 and earlier	v1.19 and earlier	320 MHz	280 MHz	280 MHz	v1.07 and earlier	250 MHz
v13.3 and later	v1.20 and later	320 MHz	280 MHz	280 MHz(1)	v1.08 and later	150 MHz

Notes:
1. The data sheet was updated to this value in v3.0, October, 2011.

Products Affected

This notice applies to all Spartan-6 LX and LXT FPGAs. The products affected include all standard part numbers and specification control document (SCD) versions of these standard part numbers. General purpose XC devices, Automotive XA devices, and Aerospace & Defense Spartan-6Q devices are affected. There are no changes to the silicon related to this change; the updated specifications apply to all production silicon.

Key Dates

These changes are effective upon this PCN release.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support http://www.xilinx.com/support/techsup/tappinfo.htm.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (http://www.xilinx.com/support). Register today and personalize your "Documentation and Design Advisory Alerts" area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: http://www.xilinx.com/support/answers/18683.htm.

Additional Documentation

Spartan-6 FPGA Data Sheet: DC and Switching Characteristics:
http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf.
Design Advisory for Spartan-6 FPGA Speed File - Updates for DCM Phase Alignment:
http://www.xilinx.com/support/answers/44193.htm.
Design Advisory for Spartan-6 FPGA Speed File - Updates for Block RAM F_{MAX} in Lower Power -1L Devices:
http://www.xilinx.com/support/answers/44192.htm.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/17/11	1.0	Initial release.

Notice of Disclaimer